Code No.: **54306** MR 15

MALLA REDDY ENGINEERING COLLEGE (AUTONOMOUS)

(Affiliated to JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD)
Gundlapochampally (H), Maisammaguda (V), Medchal (M), Medchal-Malkajgiri (Dist), Hyderabad.

M.Tech II Semester Supplementary Examinations, DECEMBER-2017

SUBJECT: **Embedded Networking**

Branch/Specialization: **ECE/Embedded Systems.**

Time: 3 hours **Max. Marks: 60**

PART – A

Answer All Questions **5 x 4Marks=20 Marks**

1) What are the features of fire wire? (4M)
2) What is USB ? How many types of data rates did USB support? (4M)
3) What is the functionality of an IP layer? (4M)
4) What are the requirements for a computer to send a message using TCP/UDP in an ether network. (4M)
5) What is coarse-grained and fine-grained node localization approach. (4M)

PART-B

Answer any five of the following questions **5 x 8 Marks= 40 Marks**

1. Write Short notes on
   a. SPI (4M)
   b. I2C (4M)
2. Explain different types of CAN bus termination methods. (8M)
3. Write a short notes on a) Twisted-pair cable. b) Fiber-optic cable c) co-axial cable. (8M)
4. a) Explain the concepts of serving web-pages with dynamic data. (4M)
   b) Explain the protocols for serving web-pages? (4M)
5. Explain data-centric routing approaches? (8M)
6. a) Mention some serial communication protocols. (4M)
   b) What are the specifications of PCI bus. (4M)
7. a) Explain how an IP address is assigned to a hosts.. (4M)
   b) What is Device Controller, Explain? (4M)
8. Write Short notes on any **two** of the following
   a. functionality of SEAD? (4M)
   b. A server side include directives? (4M)
   c. ICMP (4M)

Code No.: **54115** MR 15

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M.Tech II Semester Supplementary Examinations, DECEMBER-2017

SUBJECT: **Digital Signal Processors And Architectures**

Branch/Specialization: **ECE/Common to Embedded Systems & DS&CE**

Time: 3 hours **Max. Marks: 60**

PART – A

Answer All Questions **5 x 4Marks=20 Marks**

1. Calculate the dynamic range and precision of 48-bit double precision fixed-point format.
2. What are guard bits of ALU in dsp processor.
3. Give the syntax of MPY instruction of TMS320C54XX processors.
4. Compare the features of TMS320C54xx and ADSP 21xx processor.
5. Explain the significance of DMA sub-register addressing technique.

PART-B

Answer any five of the following questions **5 x 8 Marks= 40 Marks**

1. a) The signal sequence x[n]=[0 2 4 6 8] is interpolated using the interpolation filter sequence b_k=[0.5 1 0.5] and interpolation factor is 2. Determine the interpolated sequence y(m).
   b) Explain the block-floating point representation format with an example.

2. a) Explain Braun multiplier for signed numbers.
   b) Identify the addressing modes of the operands in each of the following instructions :
   (i) ADD B (ii) ADD 5678h
   (iii) ADD + *addrreg (iv) ADD *addrreg, offsetreg –

3. a) Draw the block diagram of indirect addressing mode for TMS320C54XX processors.
   b) Describe the operation of the following MPY and MAC instructions.
   (i) MPY 13, B (ii) MAC *AR5+,#1234H,A

4. a) Draw the architectural block diagram of ADSP 21xx processor.
   b) Explain the register file of Blackfin processor with neat diagram.

5. a) Explain the external memory interface of TMS320C5416 processor with timing diagram.
   b) Design an interface to connect a 64K x 16 flash memory to a TMS320C54xx device. The processor address is A0-A15.

6. a) What is role of a shifter in DSP? Explain the implementation of 4-bit shift right barrel shifter with a diagram.
   b) Explain the pipeline operation of TMS320C54xx processor.

7. a) Give the specifications of on-chip memory of TMS32054xx processor.
   b) Write a program to perform filtering using multiply and accumulate in indirect addressing mode. $Y(n) = h_0x(n) + h_1x(n-1) + h_2x(n-2)$

8. Write any **Two**
   a) Programmed I/O b) Saturation logic c) Interrupts of TMS32054xx processor

Code No.: **54307** MR 15

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M.Tech II Semester Supplementary Examinations, DECEMBER-2017

SUBJECT: **Sensors and Actuators**

Branch/Specialization: **ECE/Embedded Systems.**

Time: 3 hours **Max. Marks: 60**

PART – A

Answer All Questions **5 x 4Marks=20 Marks**

1. What do you mean by a smart sensor?
2. Explain about Acoustic Temperature sensor?
3. Explain about Synchro-resolvers ?
4. How smart sensor works for Connecting and Testing the LCD ?
5. What are Process control valves, explain in detail.

PART-B

Answer any five of the following questions **5 x 8 Marks= 40 Marks**

1. What is the principle behind working of Stress Sensors and write the application of these sensors
2. Explain in detail about Spectroscopic Thermometry?
3. Explain briefly how Thermal Radiation Sensors are useful in the industry.List its features
4. Explain why datacommunication is important in sensor interface explain with a neat diagram
5. How Electromagnetic Flowmeter is facilitated with Switching Magnetic Sensors SQUID Sensors
6. a. List the features for Standards required for Smart Sensor Interface and the Automation
   b. Write about linear sensor properties?
7. a. What are various blocks in mechanical actuation system, explain in detail
   b. What are Geiger Counters and where it is used?
8. Answer any **TWO**
   a. solenoids
   b. Concentration polarization
   c. Spectroscopic Thermometry

Code No.: **54119**

MR 15

MALLA REDDY ENGINEERING COLLEGE (AUTONOMOUS)

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Gundlapochampally (H), Maisammaguda (V), Medchal (M), Medchal-Malkajgiri (Dist), Hyderabad.

M.Tech II Semester Supplementary Examinations, DECEMBER-2017

SUBJECT: **System on Chip Architecture**

Branch/Specialization: **ECE/Embedded Systems.**

Time: 3 hours **Max. Marks: 60**

PART – A

Answer All Questions **5 x 4Marks=20 Marks**

1. What are the different types of sources?
2. Differentiate parallel and pipeline processing approaches?
3. Write advantages, disadvantages and applications of CMOS
4. What is multiplication and draw the architecture of multiplier?
5. Define DRAM

PART-B

Answer any five of the following questions **5 x 8 Marks= 40 Marks**

1. Explain (a) Surface scattering 4M
   (b) Hot electron 4M
2. What do you mean by pipelining and parallel processing approaches 8M
3. (a) Explain CMOS adder's architecture 4M
   (b) Writ a short note on low voltage low power logic styles 4M
4. Briefly explain about
   (a) Braun multiplier 4M
   (b) Booth multiplier 4M
5. Explain following terms
   (a) SRAM 4M
   (b) DRAM 4M
6. (a) Explain VTCMOS circuit 4M
   (b) What are the different sources of power dissipations? 4M
7. (a) Briefly explain about multiplier architecture 4M
   (b) Write a short note on carry save adder? 4M
8. Explain
   (i) Leakage power dissipation 4M
   (ii) System level measurement 4M

2. a) write about split - I and D - caches ? (8M).

4. a) Explain and draw the interconnect architecture ? (4M)

b) write short notes on trade off analysis ? (4M)

Code No.: **54104** MR 15

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M.Tech II Semester Supplementary Examinations, DECEMBER-2017

SUBJECT: **Hardware and Software Co-Design**

Branch/Specialization: **ECE/Embedded Systems.**

Time: 3 hours **Max. Marks: 60**

PART – A

Answer All Questions **5 x 4Marks=20 Marks**

1. Distinguish between design specification and verification.
2. Explain reactive system co-synthesis with reference to distributed system co- synthesis.
3. Discuss about the needs of embedded software development.
4. Distinguish between Design verification and Implementation verification.
5. Explain Heterogeneous specification.

PART-B

Answer any five of the following questions **5 x 8 Marks= 40 Marks**

1. Explain the following portioning algorithms.
   a) Cosyma b). Vulan

2. a). Discuss about prototyping and emulation environments.
   b). Distinguish between control-dominated system and data-dominated systems.

3. Explain in detail about various compilation techniques and tools available for embedded processor architectures.

4. Define the terms and explain them in brief
   a).Design and Co-design.
   b). Interface verification.

5. Explain the following with respect to languages for system-level specification and design.
   a). System level specification languages.
   b). Multi language Co-simulation.

6. a. Explain in detail, the Hierarchical Concurrent Finite State Machine (HCFSM) model
   b. Explain Architecture specialization techniques with suitable example.

7. a).Explain any one of advanced embedded processor architecture with appropriate figure.
   b). what is meant by coordinating concurrent computations? Explain.

8. Answer any **TWO**
   a). source debugging
   b).Compiler validation
   c).Hardware-software

Code No.: **54124**

MR 15

MALLA REDDY ENGINEERING COLLEGE (AUTONOMOUS)

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Gundlapochampally (H), Maisammaguda (V), Medchal (M), Medchal-Malkajgiri (Dist), Hyderabad.

M.Tech II Semester Supplementary Examinations, DECEMBER-2017

SUBJECT: **AD Hoc Wireless Networks**

Branch/Specialization: **ECE/Embedded Systems.**

Time: 3 hours **Max. Marks: 60**

PART – A

Answer All Questions **5 x 4Marks=20 Marks**

1. Writs the major differences between wireless LAN and wired LAN.
2. Write the design goals of a MAC protocol for Ad Hoc Wireless networks.
3. Write the issues in designing routing protocols for Ad Hoc Wireless Networks.
4. Discuss the Transmission management schemes
5. Explain the Location Discovery in wireless Sensor Networks.

PART-B

Answer any five of the following questions **5 x 8 Marks= 40 Marks**

1. Explain the IEEE 802.11 Wireless LAN Architecture.
2. Explain MACA by invitation protocol and medium access with reduced handshake protocol.
3. Discuss the major challenges in designing a Routing Protocol for Ad hoc wireless networks.
4. Discuss the Network layer solutions in providing QOS for Ad Hoc Wireless Networks.
5. Explain the MAC Protocols for Sensors Networks
6. a. Discuss the issues in designing MAC protocol for Ad Hoc Wireless networks.
   b. Write about Application controlled transport protocol (ACTP)
7. a. Explain the Hierarchical routing protocol.
   b. List the reasons why TCP does not perform well in Ad Hoc wireless networks.
8. Answer any **TWO**
   a. Mobile IP
   b. Explain the MAC protocol that uses Directional antennas.
   C. Explain the system power management schemes.